MY10N40T

400V N-Channel Enhancement Mode MOSFET

MAOYUANWEI semiconductor

General Description

The MY10N40T N-channel enhanced vdmosfets, is obtained by the self-aligned planar technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. Which accords with the RoHS standard

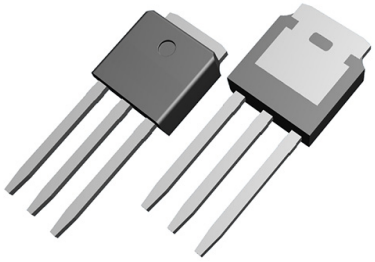
RoHS Compliant

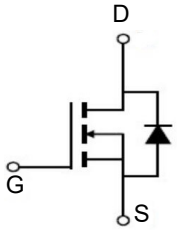
Features

V_{DSS}	400	V
I_D	10	A
P_D(T_C= 2 5 ℃)	100	W
$R_{DS(ON)}$(atV_{GS} =10V)	<0.55	Ω

Application

- Fast switching
- Low on-resistance
- ULow gate charge and input capacitance
  100% avalanche tested





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY10N40T	TO-251	10N40	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter		Symbol	MY10N40T	Unit
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C=25°C T_C=100°C	I_D	10 6.3	A
Pulsed Drain Current (Note 1)		I_{DM}	40	A
Single Pulse Avalanche Energy(Note 2)		E_{AS}	450	mJ
Avalanche Current(Note 1)		I_{AR}	-	A
Power Dissipation T_C=25°C		P_D	100	W
Operating Junction and Storage Temperature		T_J/T_{STG}	-55~+175	℃

Gate-Source Voltage

Parameter	Symbol	MY10N40T	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal resistance Junction to Case	$R_{\theta JC}$	1.25	°C/W

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	400	-	-	V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=400V,V_{GS}=0V	-	-	1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V	-	-	100	nA
	Reverse		V_{GS}=-30V,V_{DS}=0V	-	-	-100	nA
On Characteristics(Note 4)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	2.0	3.0	4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=5A	-	0.44	0.55	Ω
Dynamic Characteristics(Note 5)							
Input Capacitance		C_{ISS}	V_{DS}=25V,V_{GS}=0V,f=1MHz	-	1126	-	pF
Output Capacitance		C_{OSS}		-	124	-	pF
Reverse Transfer Capacitance		C_{RSS}		-	8	-	pF
Switching Characteristics (Note 5)							
Turn-On Delay Time		td(on)	V_{DD}=200V,I_D=10A, R_G=10Ω	-	18	-	ns
Turn-On Rise Time		t_R		-	23	-	ns
Turn-Off Delay Time		td(off)		-	41	-	ns
Turn-Off Fall Time		tf		-	19	-	ns
Total Gate Charge		Q_G	V_{DD}=320V,I_D=10A, V_{GS}=10V	-	23	-	nC
Gate-Source Charge		Q_{GS}		-	5.2	-	nC
Gate-Drain Charge		Q_{GD}		-	8.5	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_S=10A	-	-	1.5	V
Maximum Continuous Drain-Source Diode Forward Current		I_S		-	-	10	A
Reverse Recovery Time		trr	V_{GS}=0V, I_F=10A dI$_F$/dt=100A/μs (Note 1)	-	376	-	ns
Reverse Recovery Charge		Q_{RR}		-	2560	-	nC

Notes : 1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L=10mH, I_D=9.5A,V_{DD}=50V,Starting T_J=25°C
4 Pulse Test: Pulse width ≤300μS, Duty cycle≤2%
5 Guaranteed by design,not subject to production

Typical Characteristics

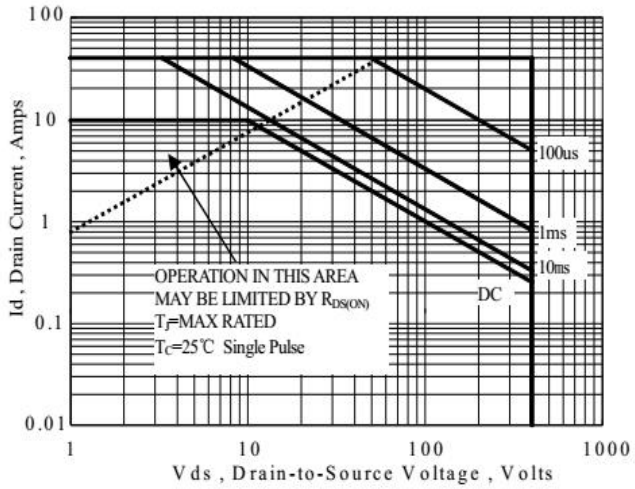


Figure 1 Maximum Forward Bias Safe Operating Area

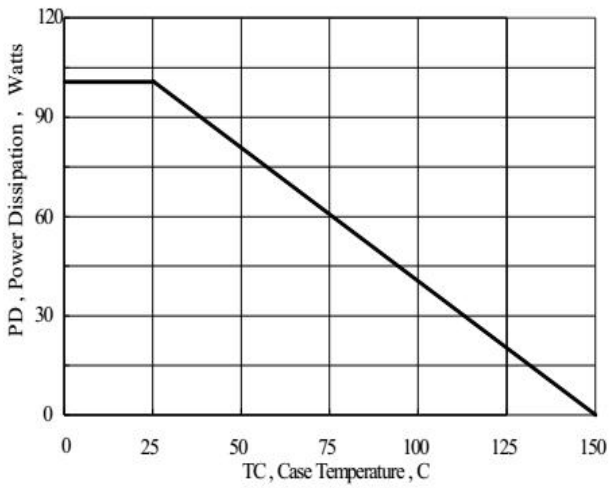


Figure 2 Maximum Power Dissipation vs Case Temperature

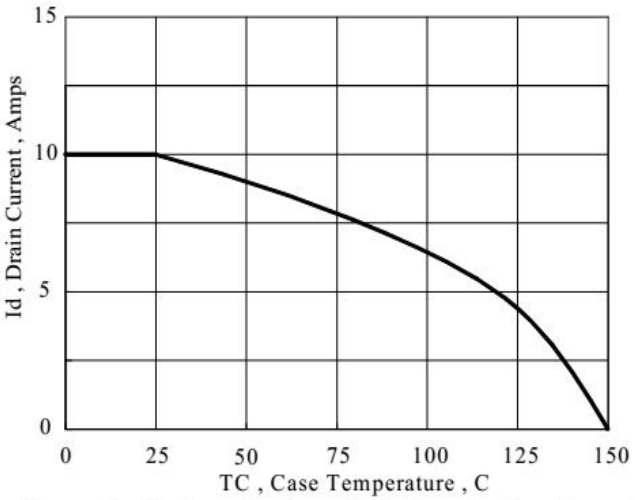


Figure 3 Maximum Continuous Drain Current vs Case Temperature

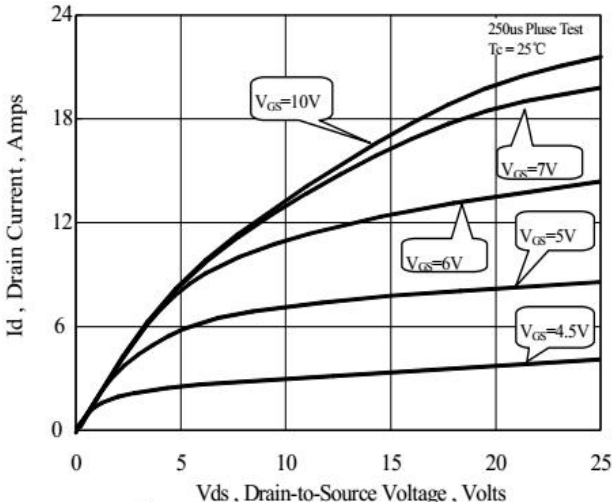


Figure 4 Typical Output Characteristics

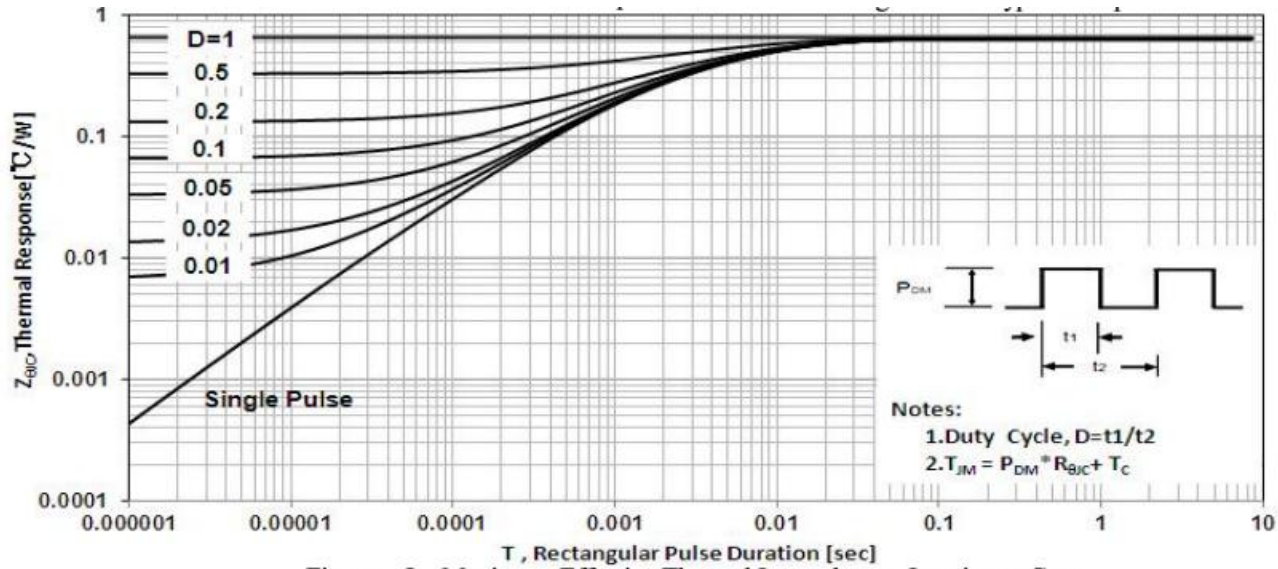


Figure 5 Maximum Effective Thermal Impendance , Junction to Case

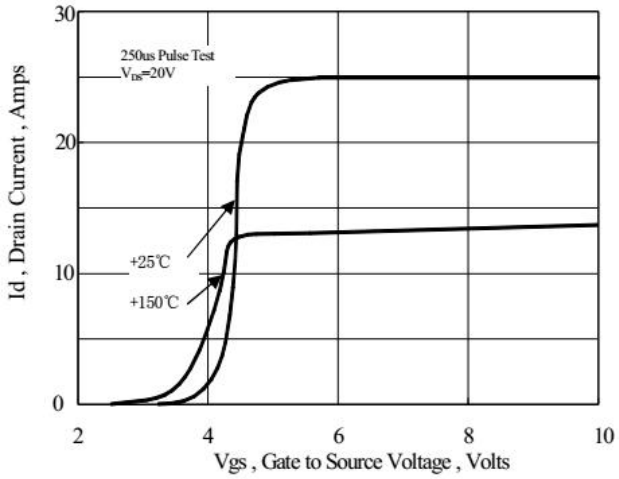


Figure 6 Typical Transfer Characteristics

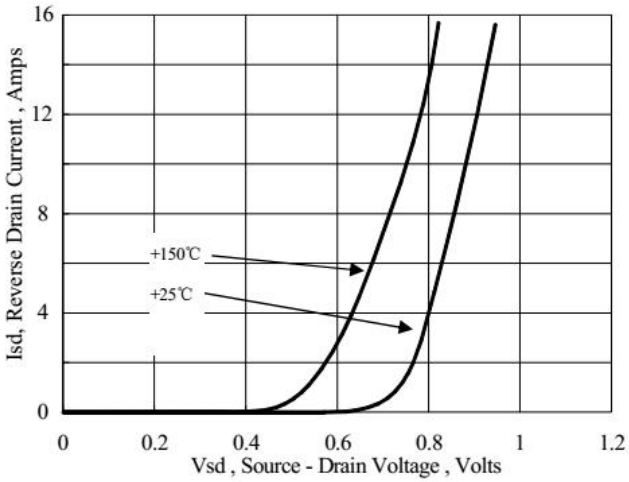


Figure 7 Typical Body Diode Transfer Characteristics

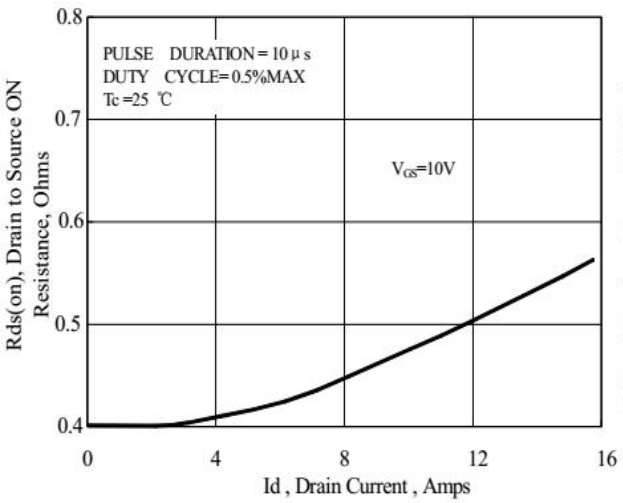


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

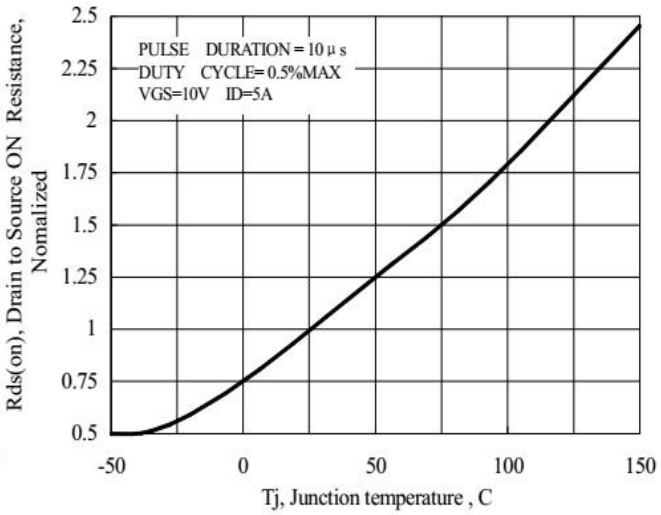


Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

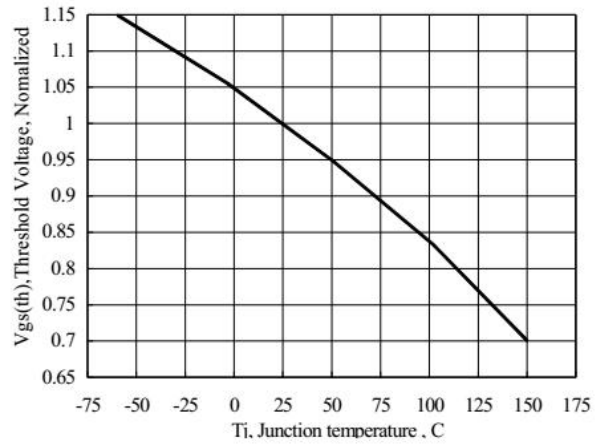


Figure 10 Typical Theshold Voltage vs Junction Temperature

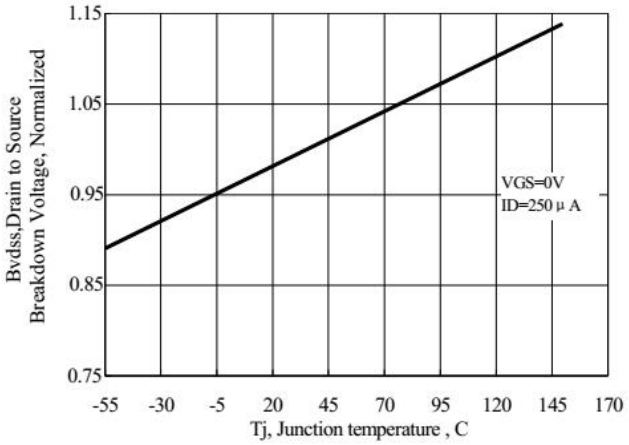


Figure 11 Typical Breakdown Voltage vs Junction Temperature

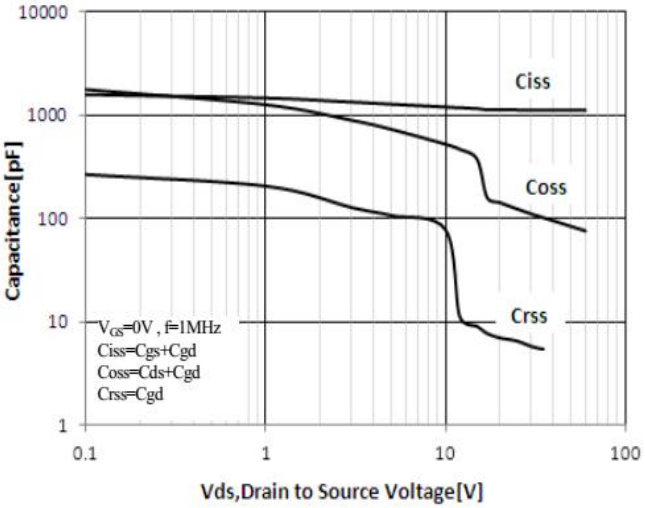


Figure 12 Typical Capacitance vs Drain to Source Voltage

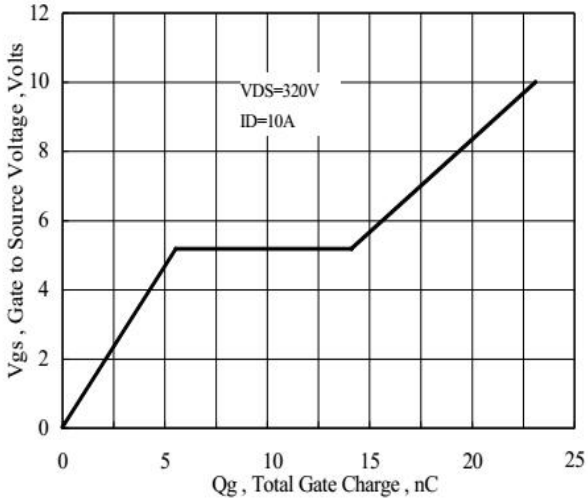


Figure 13 Typical Gate Charge vs Gate to Source Voltage

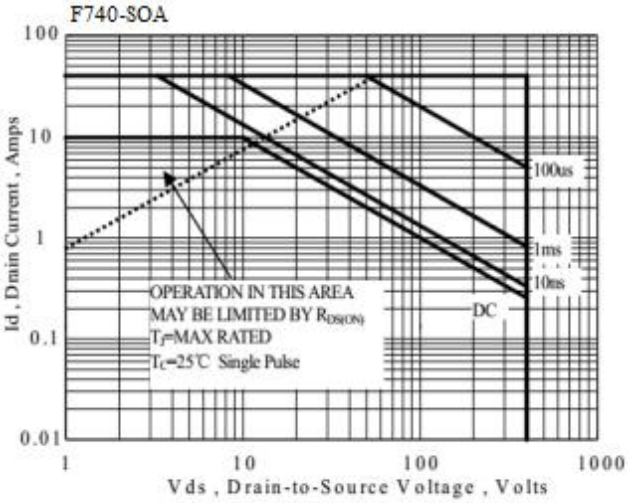


Figure 14 Maximum Forward Bias Safe Operating Area

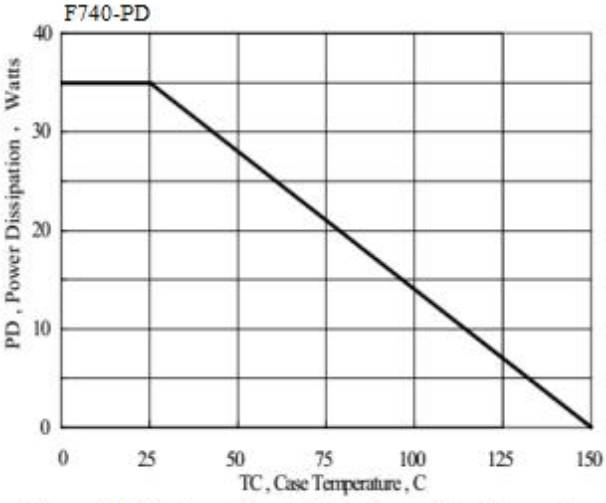


Figure 15 Maximum Power Dissipation vs Case Temperature

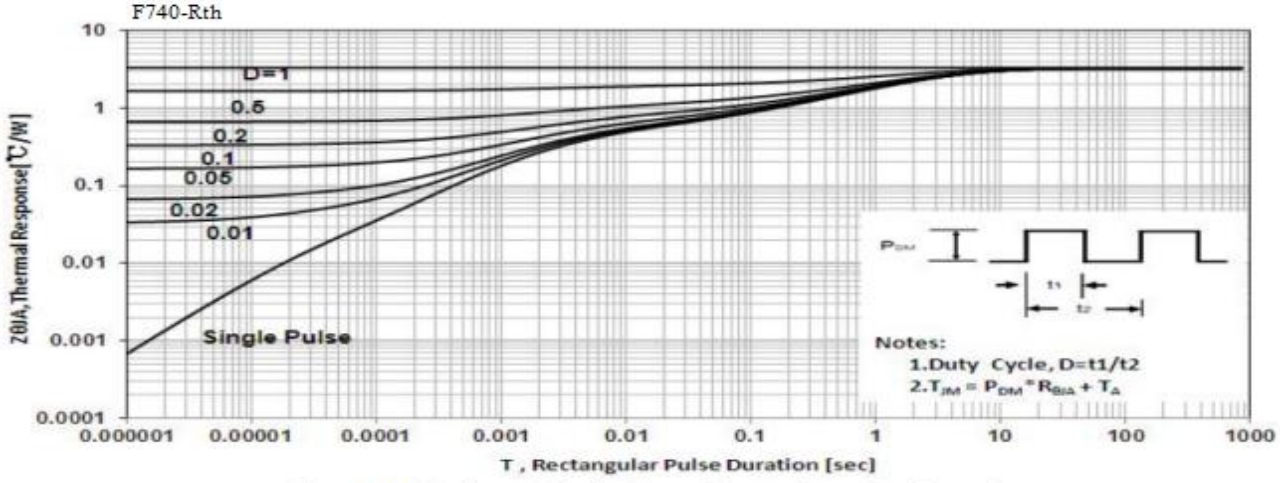
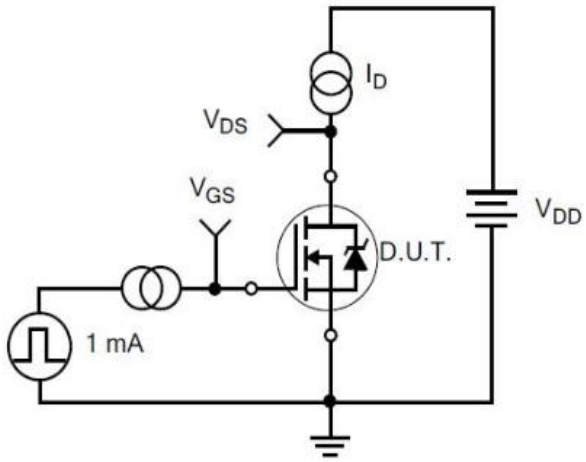
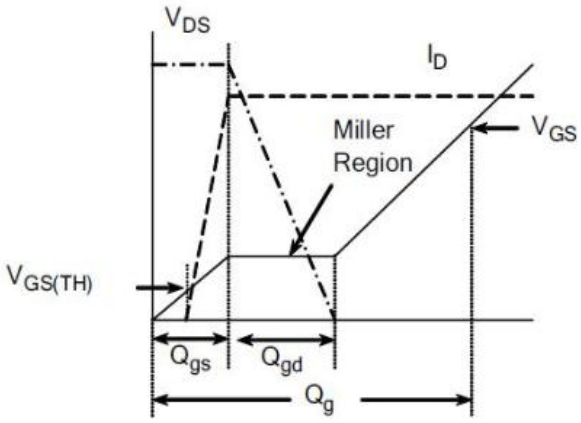


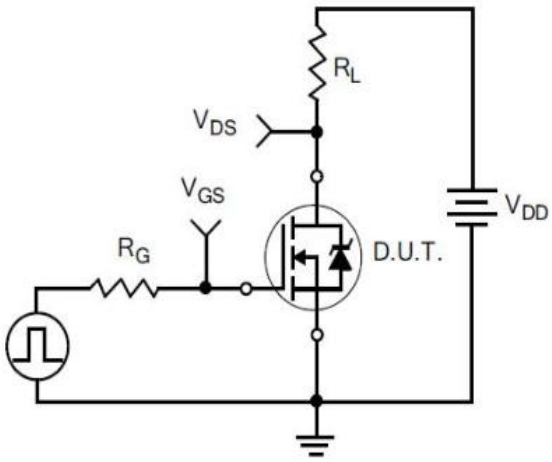
Figure 16 Maximum Effective Thermal Impendance , Junction to Case



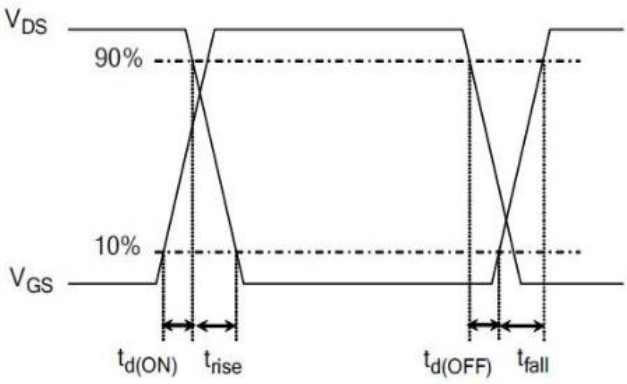
1) Gate Charge Test Circuit



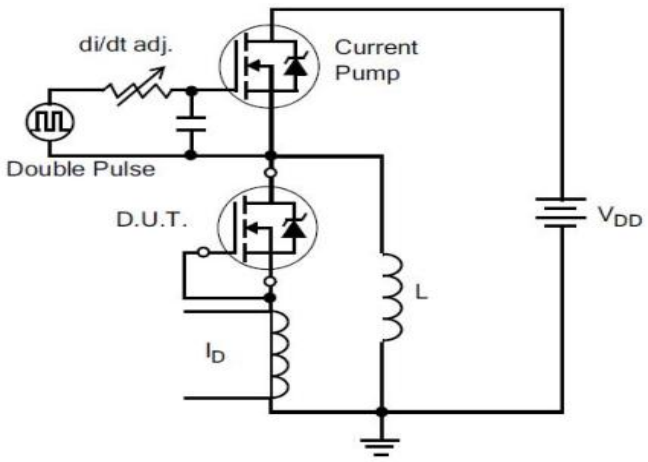
2) . Gate Charge Waveform



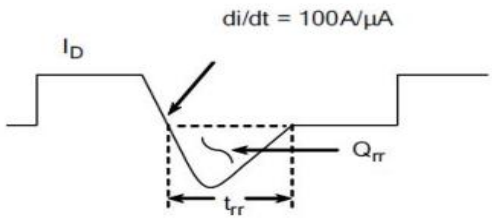
3) Resistive Switching Test Circuit



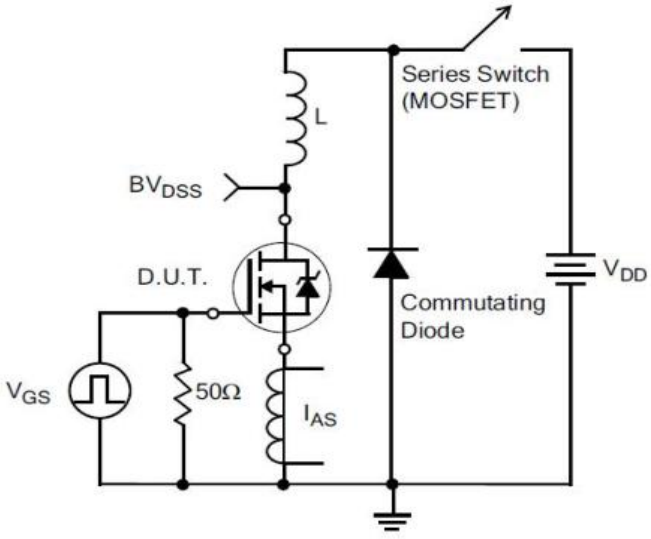
4) Resistive Switching Waveforms



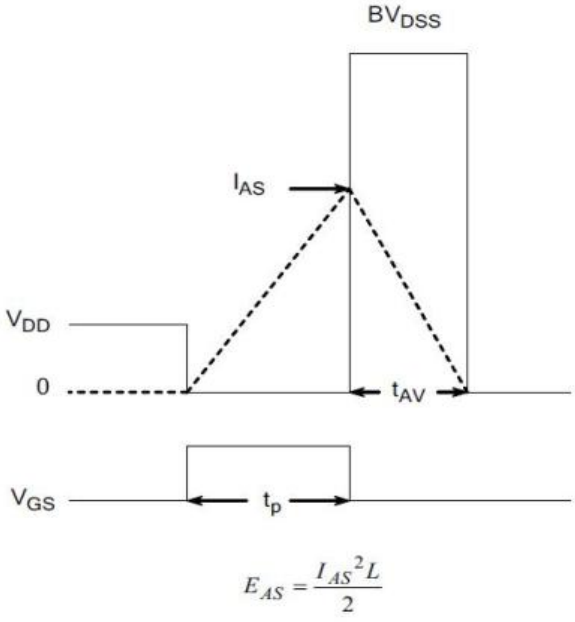
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform

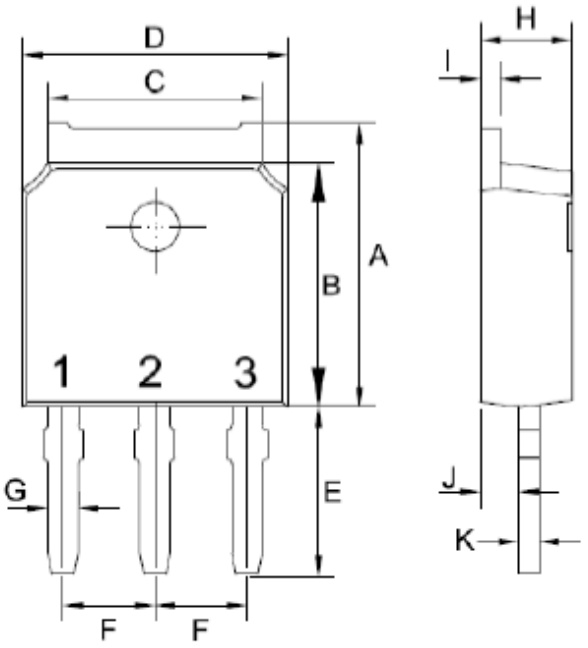


7) . Unclamped Inductive Switching Test Circuit



8) Unclamped Inductive Switching Waveforms

Package Mechanical Data-TO-251-JQ Single



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	6.85	7.25	0.270	0.285
B	5.8	6.3	0.228	0.248
C	5	5.53	0.197	0.218
D	6.3	6.8	0.248	0.268
E	3.5	4.35	0.138	0.171
F	2.19	2.39	0.086	0.094
G	0.45	0.85	0.018	0.033
H	2.2	2.4	0.087	0.094
I	0.41	0.61	0.016	0.024
J	0.71	1.31	0.028	0.052
K	0.41	0.61	0.016	0.024