General Description

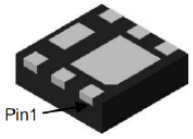
The MY1216 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

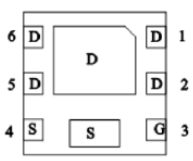
Features

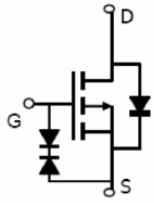
V_{DSS}	-20	V
I_D	-16	A
$R_{DS(ON)}$(atV_{GS}=10V)	15.5	mΩ
$R_{DS(ON)}$(atV_{GS}=4.5V)	22	mΩ

Application

- Battery protection
- Load switch
- Uninterruptible power supply







Schematic diagram

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY1216	PDFN2*2-6	MY1216	3000

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-16	A
Pulsed Drain Current	I_{DM}	-50	A
Maximum Power Dissipation	P_D	1.2	W
Derating factor	$R_{\theta JC}$	0.48	W/℃
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃
Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	100	℃/W

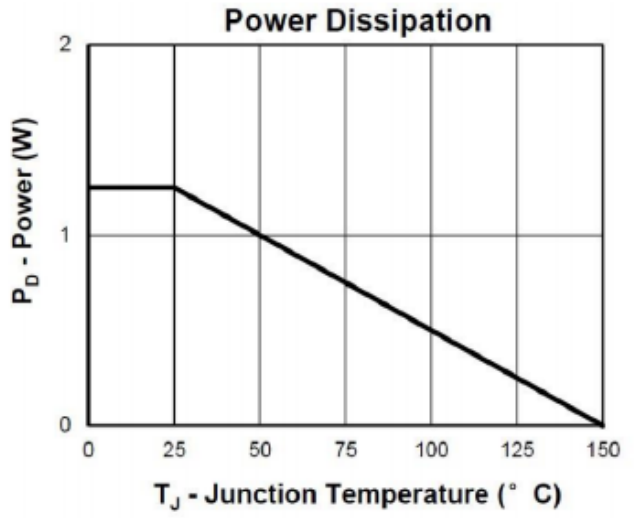
Electrical Characteristics (T_C=25 ℃, unless otherwise noted)

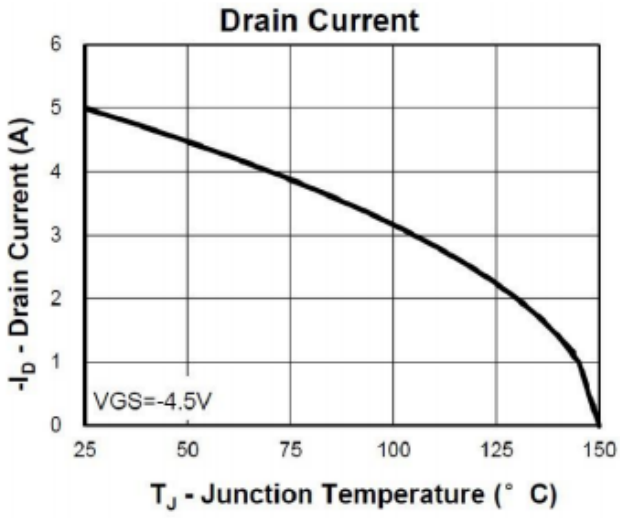
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-20	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=-20V, V_{GS}=0V	-	-	-1	μA
Gate-body leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±10V	-	-	-100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-0.4	-0.7	-1.0	V
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-15A	-	15.5	21	mΩ
		V_{GS}=-2.5V, I_D=-10A	-	22	30	
Forward transconductance	gfs	V_{GS}=-5V, I_D=-6A	-	5	-	S
Input capacitance	C_{ISS}	V_{DS}=-10V ,V_{GS}=0V f=1.0MHz	-	2100	-	pF
Output capacitance	C_{OSS}		-	498	-	
Reverse transfer capacitance	C_{RSS}		-	300	-	
Turn-on delay time	$t_{D(ON)}$	V_{DD}=-10V I_D=-2.8A V_{GEN}=-4.5V R_L=10ohm R_{GEN}=-6ohm	-	25	-	ns
Rise time	tr		-	30	-	
Turn-off delay time	$t_{D(OFF)}$		-	70	-	
Fall time	tf		-	50	-	
Total gate charge	Qg	V_{DS}=-10V,I_D=-6A V_{GS}=-4.5V	-	17	-	nC
Gate-source charge	Qgs		-	4.1	-	
Gate-drain charge	Qgd		-	4.3	-	
Diode forward voltage	V_{SD}	V_{GS}=0V,Is=-1.25A	-	-0.81	-1.2	V

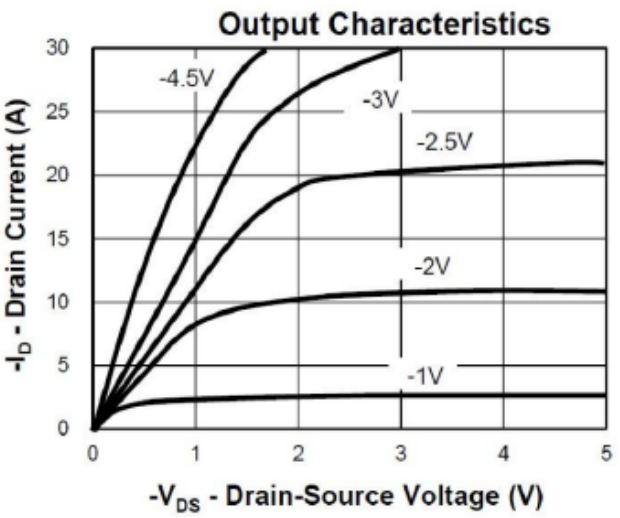
Notes:

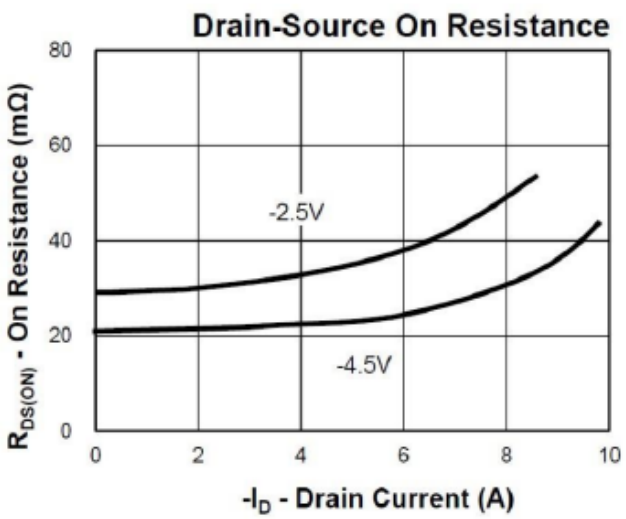
a. surface mounted on FR4 board,t≤10sec
b. pulse test: pulse width≤300μs,duty≤2%
c. guaranteed by design, not subject to production testing

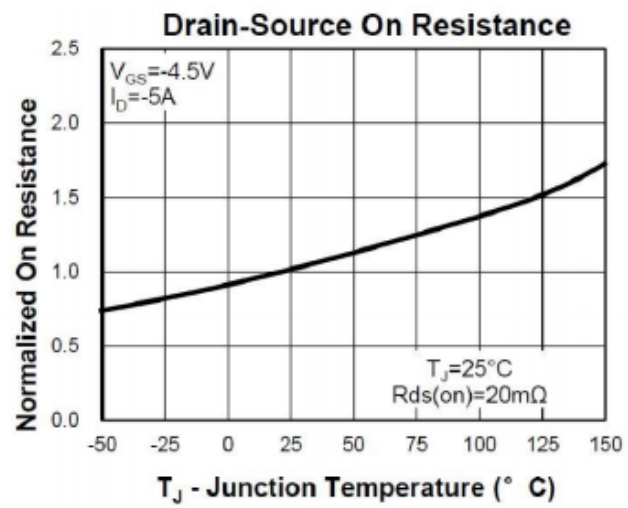
Typical Characteristics

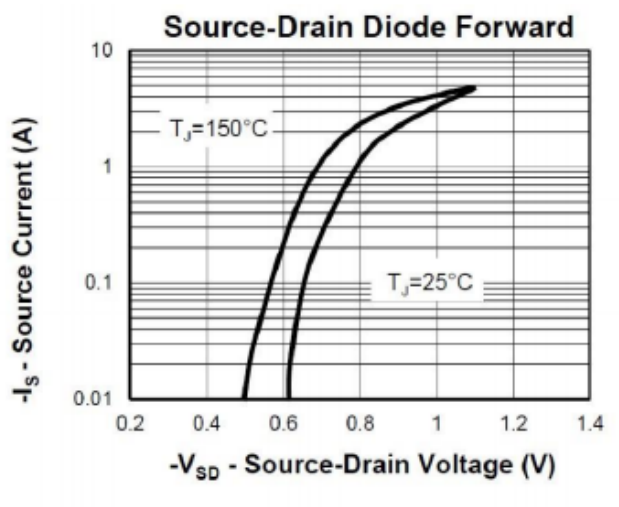


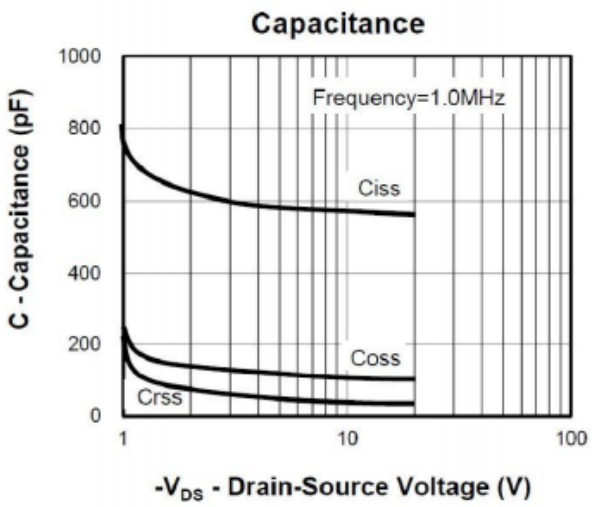


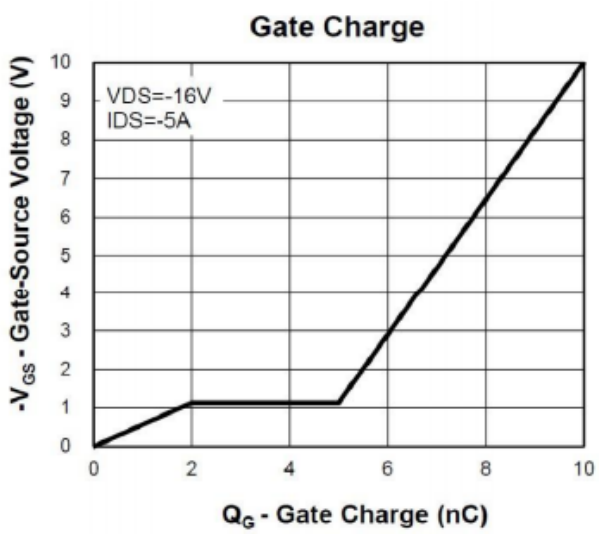


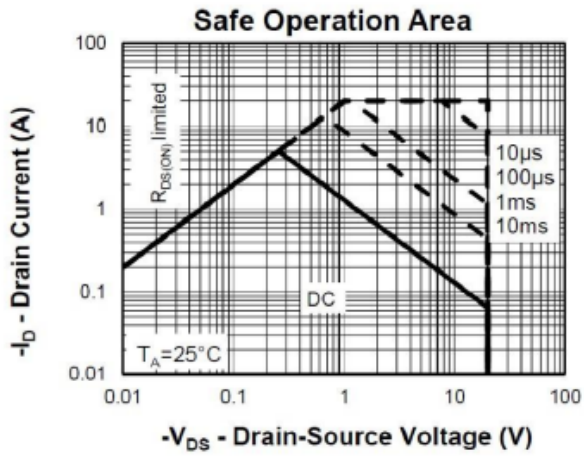


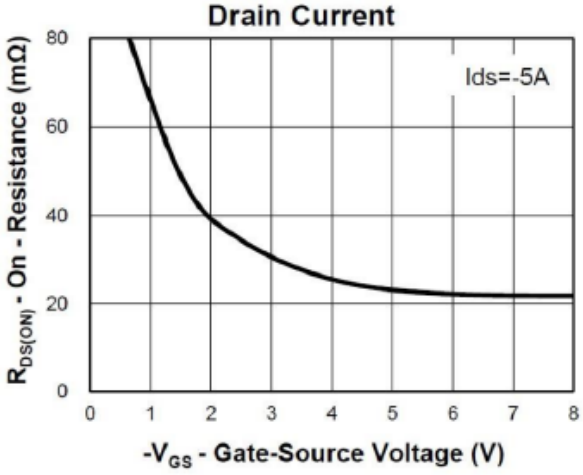


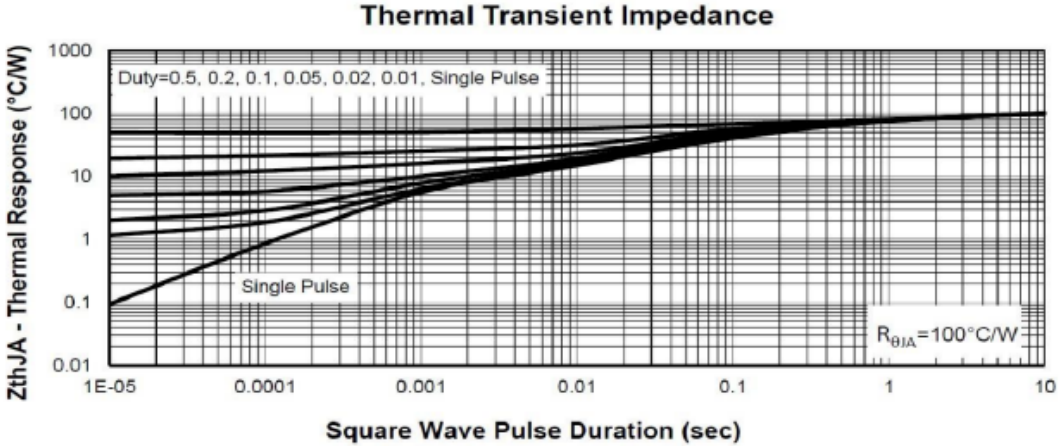



Capacitance
C - Capacitance (pF)
1000
800
600
400
200
0
Frequency=1.0MHz
Ciss
Coss
Crss
1
10
100
-VDS - Drain-Source Voltage (V)

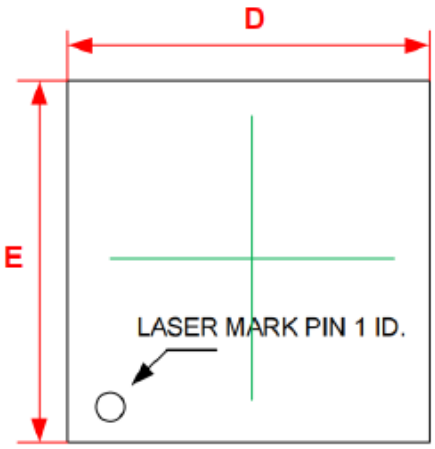

Gate Charge
-VGS - Gate-Source Voltage (V)
10
9
8
7
6
5
4
3
2
1
0
VDS=-16V
IDS=-5A
0
2
4
6
8
10
QG - Gate Charge (nC)


Safe Operation Area
-ID - Drain Current (A)
100
10
1
0.1
0.01
RDS(ON) limited
10μs
100μs
1ms
10ms
DC
TA=25°C
0.01
0.1
1
10
100
-VDS - Drain-Source Voltage (V)

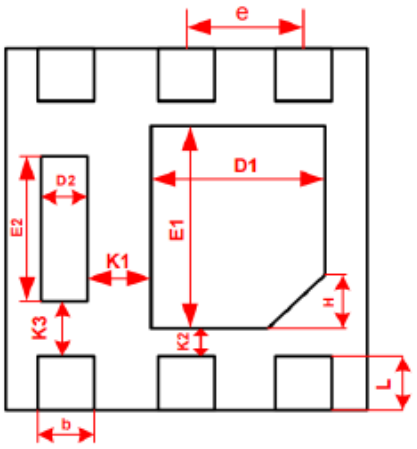

Drain Current
RDS(ON) - On - Resistance (mΩ)
80
60
40
20
0
Ids=-5A
0
1
2
3
4
5
6
7
8
-VGS - Gate-Source Voltage (V)


Thermal Transient Impedance
ZthJA - Thermal Response (°C/W)
1000
100
10
1
0.1
0.01
Duty=0.5, 0.2, 0.1, 0.05, 0.02, 0.01, Single Pulse
Single Pulse
RθJA=100°C/W
1E-05
0.0001
0.001
0.01
0.1
1
10
Square Wave Pulse Duration (sec)

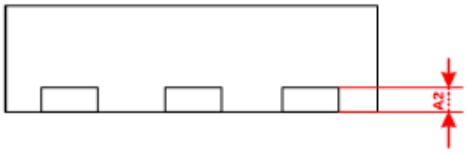
Package Mechanical Data-DFN2*2-6L-8JQ Single



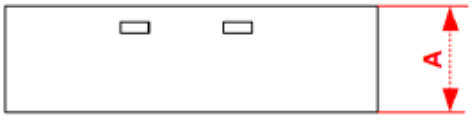
TOP VIEW



BOTTOM VIEW



SIDE VIEW



SIDE VIEW

Common Dimension (mm)			
PKG	DFN2020-6L-B		
SYMBOL	MIN.	MON.	MAX.
A	0.413	0.452	0.493
A2		0.127REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D1	0.85	0.95	1.05
E1	1.05	1.15	1.25
D2	0.20	0.25	0.30
E2	0.69	0.79	0.89
e	0.55	0.65	0.75
H	0.25	0.30	0.35
K1	0.25MIN		
K2	0.15MIN		
K3	0.20MIN		
L	0.20	0.25	0.30