

General Description

The MY7G04C uses Trench Power LV MOSFET technology, High density cell design for low $R_{DS(ON)}$. This device is suitable for use as a Battery protection or High Speed switching.

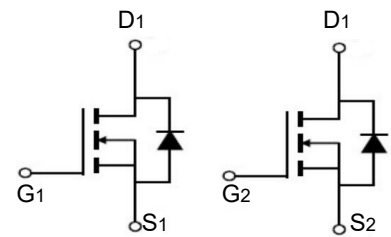
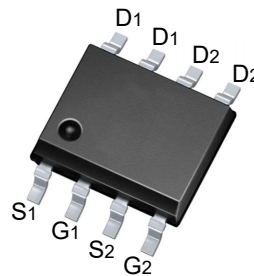


Features

V_{DSS}	40	-40	V
I_D	7	-7	A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	<37		m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<45		m Ω
$R_{DS(ON)}$ (at $V_{GS}=10V$)	<-48		m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<-68		m Ω

Applications

- Power management
- Load switch
- Wireless charger



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY7G04C	SOP-8	7G04C	3000

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage	V_{DS}	40	-40	V
Gate-source Voltage	V_{GS}	± 20	± 20	V
Drain Current	I_D	7	-7	A
Pulsed Drain Current ^A	I_{DM}	35	-30	A
Total Power Dissipation	P_D	2	2	W
Thermal Resistance Junction-to-Ambient ^B	$R_{\theta JA}$	62.5	62.5	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	-55~+150	$^\circ\text{C}$

N-Channel Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.5	3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=7A$			37	m Ω
		$V_{GS}=4.5V, I_D=6A$			45	
Diode Forward Voltage	V_{SD}	$I_S=6A, V_{GS}=0V$			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V, f=1MHz$ Z		381		pF
Output Capacitance	C_{oss}			50		
Reverse Transfer Capacitance	C_{rss}			15		
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=20V, I_D=8A$		10.3		nC
Gate-Source Charge	Q_{gs}			1.8		
Gate-Drain Charge	Q_{gd}			2.3		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V,$ $V_{DD}=20V, R_L=2.5\Omega$ $R_{GEN}=3\Omega$		4		ns
Turn-on Rise Time	t_r			18		
Turn-off Delay Time	$t_{D(off)}$			14		
Turn-off fall Time	t_f			20		

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

P-Channel Electrical Characteristics (TJ=25 °C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-40			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1	-1.5	-3	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-7A		37	48	mΩ
		V _{GS} =-4.5V, I _D =-3.5A		58	68	
Diode Forward Voltage	V _{SD}	I _S =-4.2A, V _{GS} =0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-20V, V _{GS} =0V, f=1MHZ		522		pF
Output Capacitance	C _{oss}			103		
Reverse Transfer Capacitance	C _{rss}			64		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-20V, I _D =-8A		13.3		nC
Gate-Source Charge	Q _{gs}			4.1		
Gate-Drain Charge	Q _{gd}			3.4		
Turn-on Delay Time	t _{D(on)}	V _{GEN} =-10V, V _{DD} =-20V, R _G =6Ω, R _L =2.3Ω		7.4		ns
Turn-on Rise Time	t _r			5.7		
Turn-off Delay Time	t _{D(off)}			20		
Turn-off fall Time	t _f			7		

C. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

D. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

N-Channel Typical Characteristics

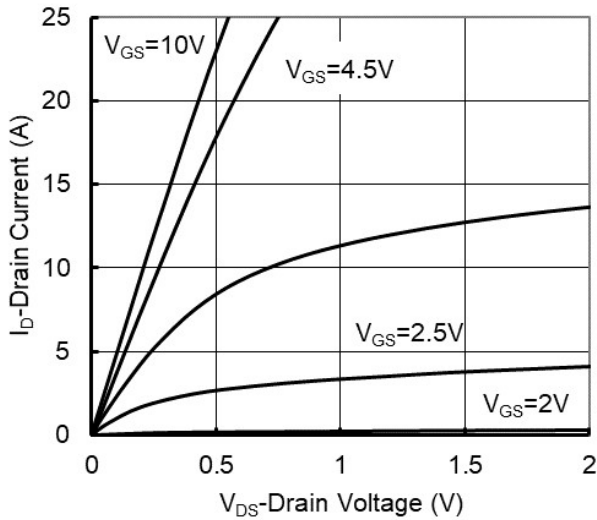


Figure1. Output Characteristics

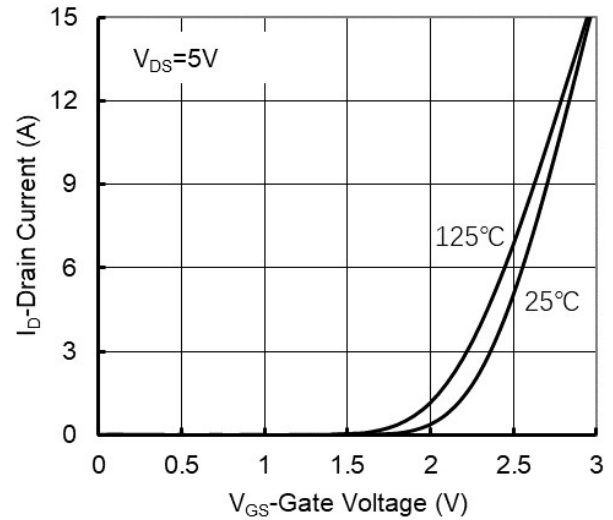


Figure2. Transfer Characteristics

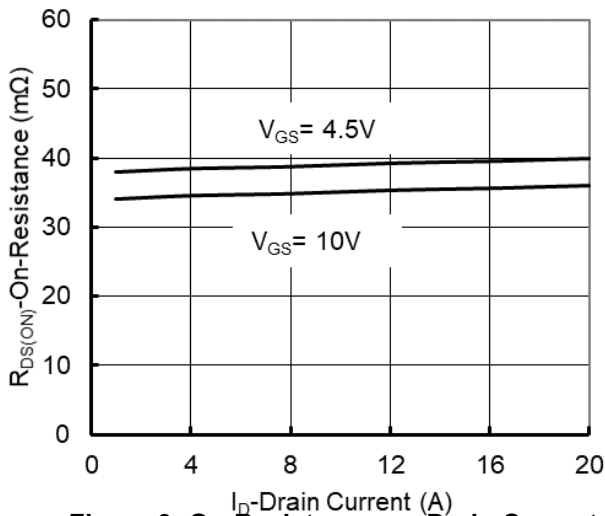


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

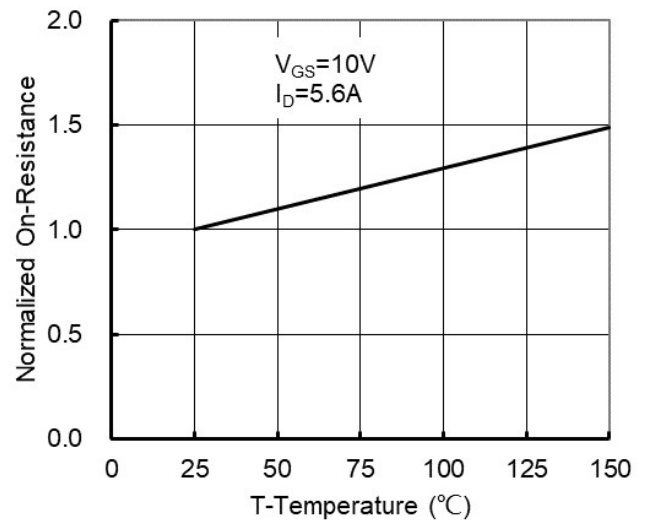


Figure 4: On-Resistance vs. Junction Temperature

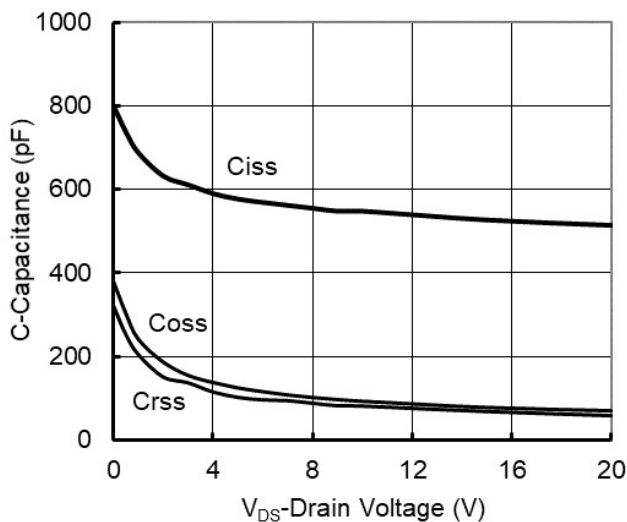


Figure5. Capacitance Characteristics

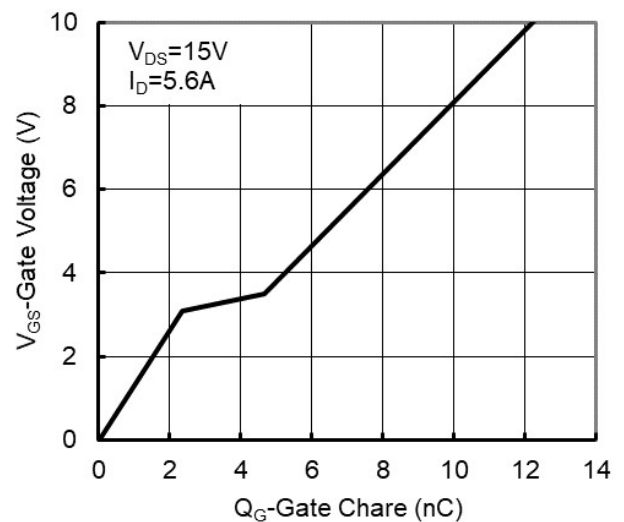


Figure6. Gate Charge

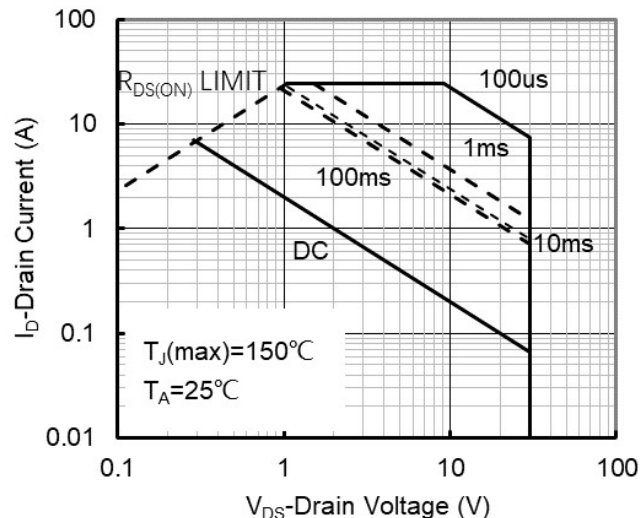


Figure7. Safe Operation Area

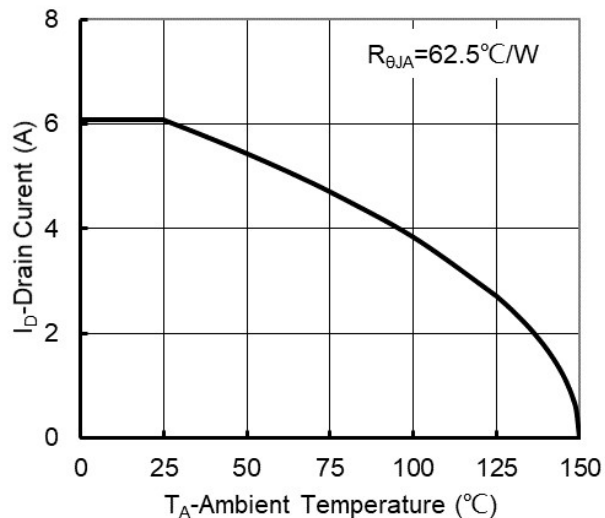


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

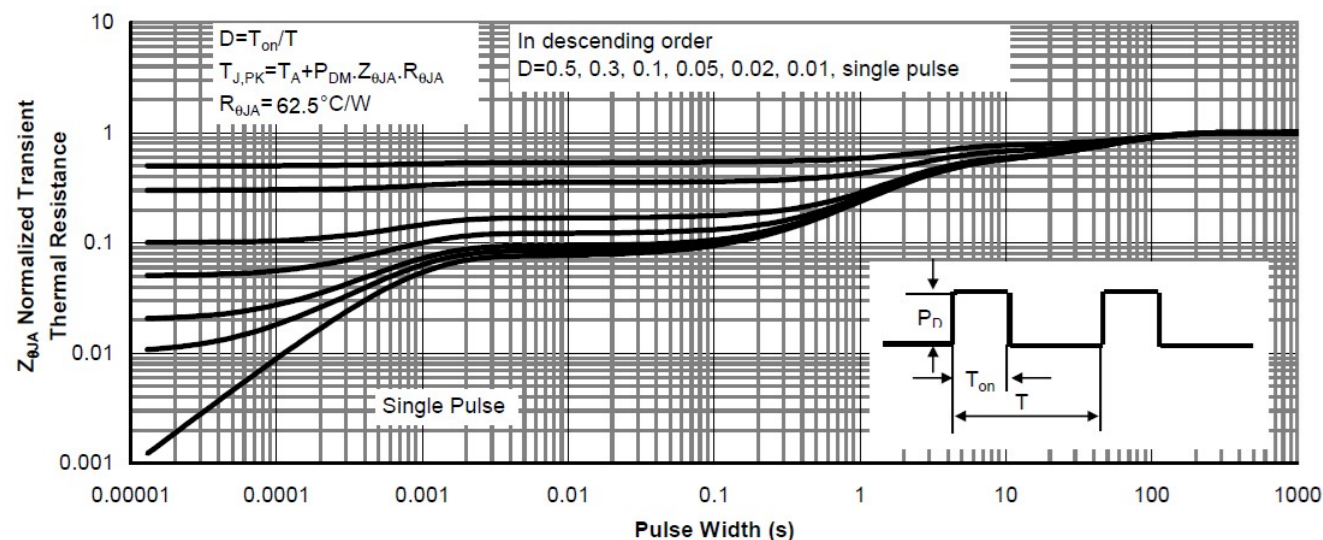


Figure9.Normalized Maximum Transient Thermal Impedance

P-Channel Typical Characteristics

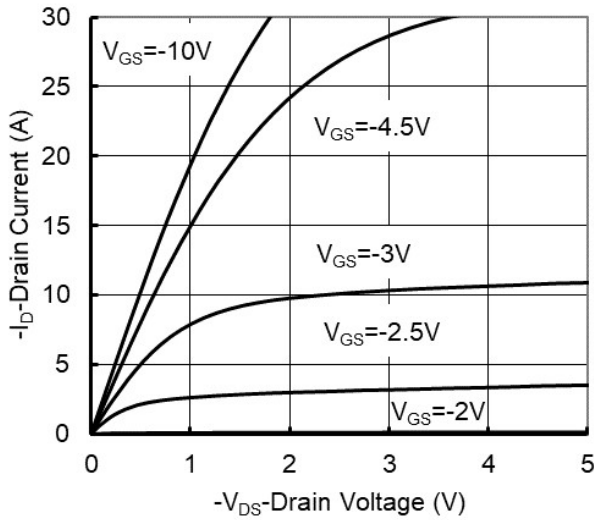


Figure1. Output Characteristics

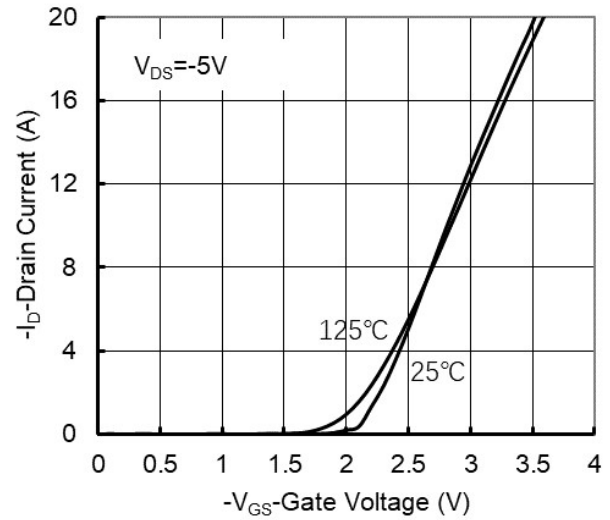


Figure2. Transfer Characteristics

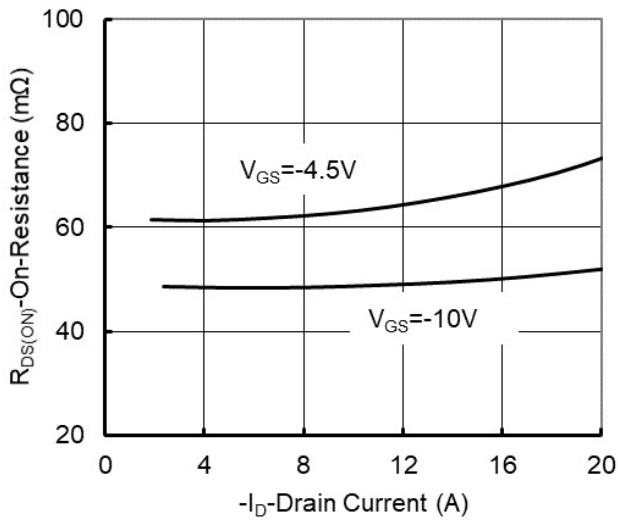


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

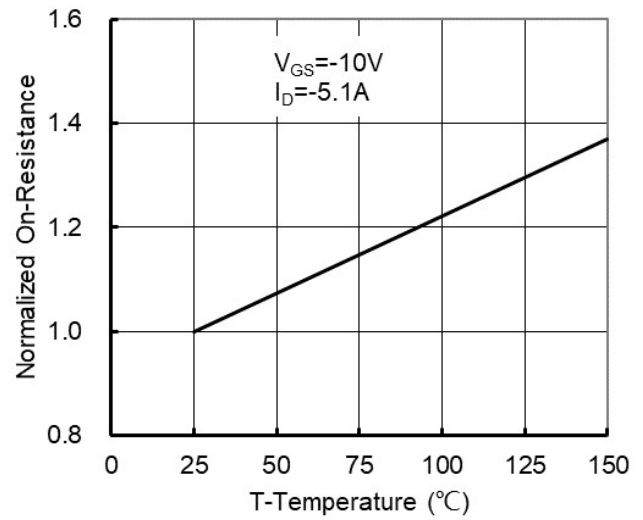


Figure 4: On-Resistance vs. Junction Temperature

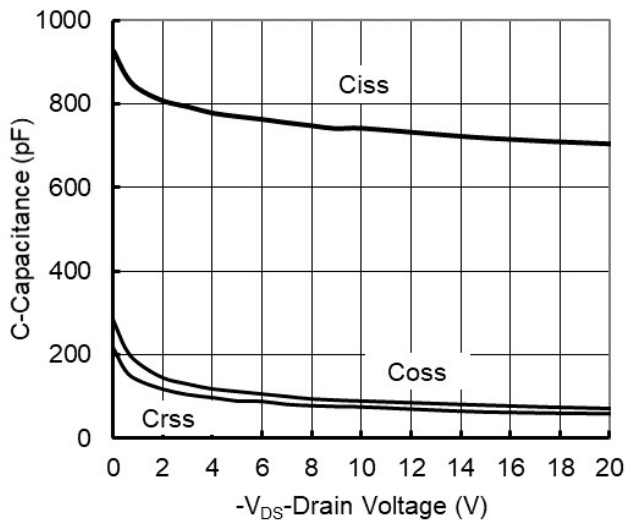


Figure5. Capacitance Characteristics

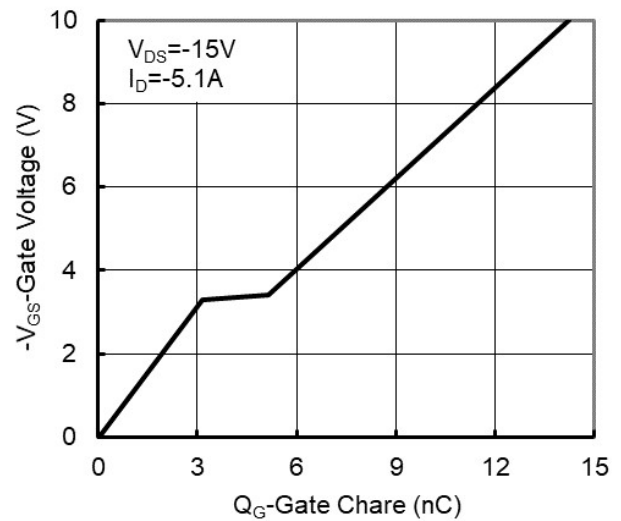


Figure6. Gate Charge

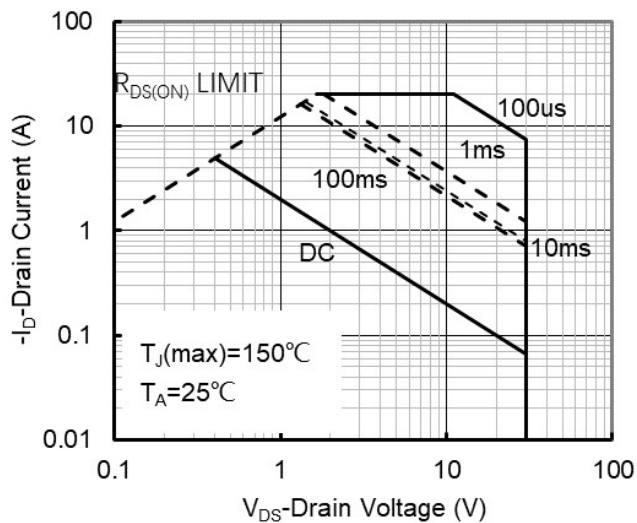


Figure7. Safe Operation Area

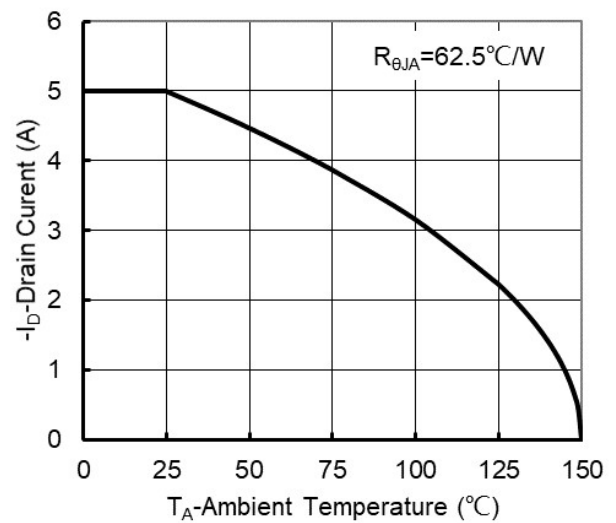


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

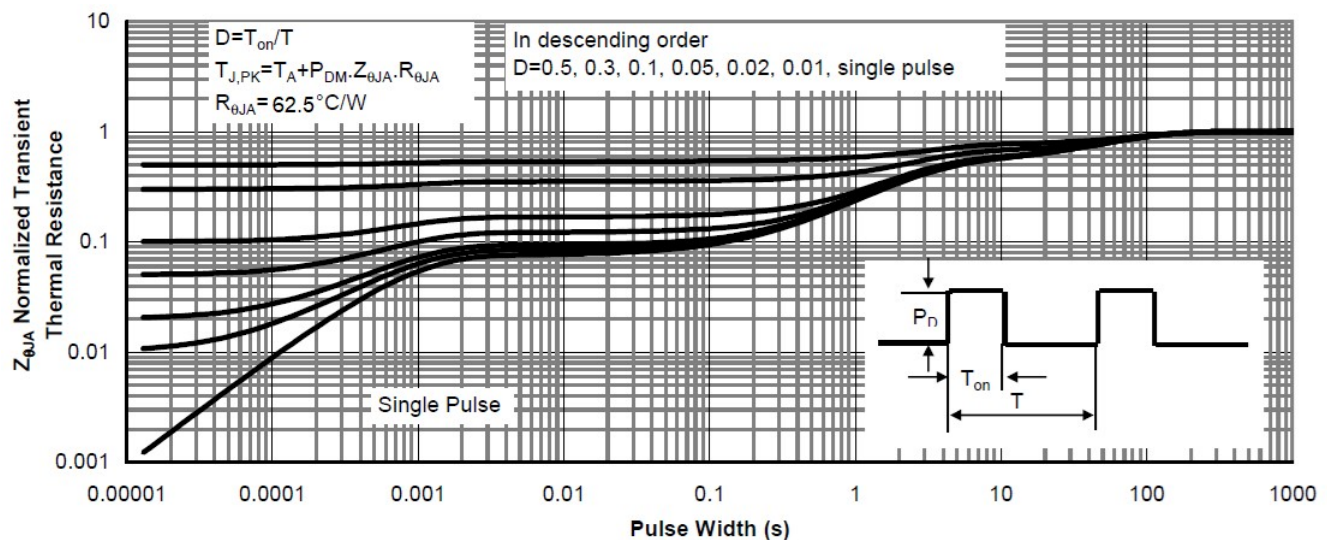
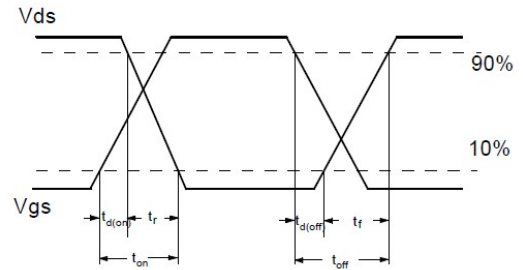
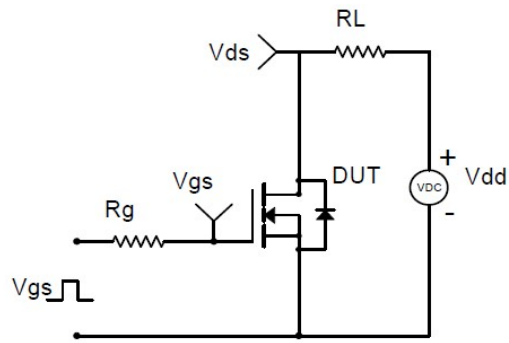
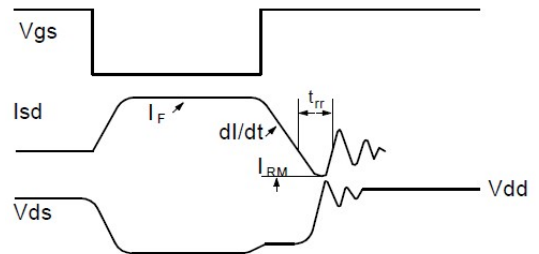
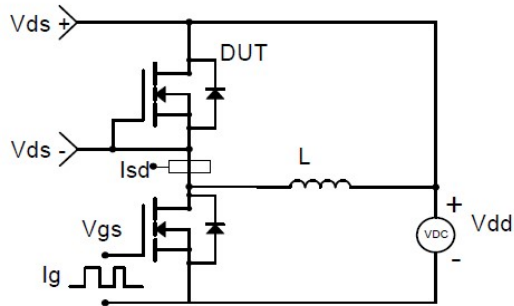


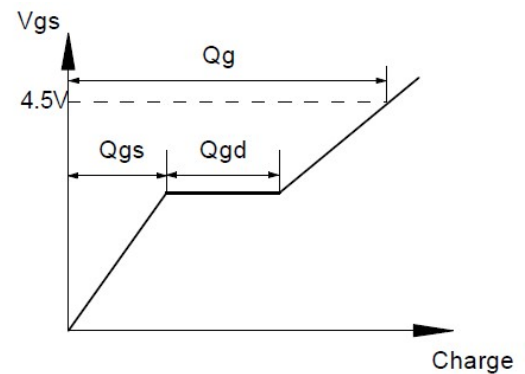
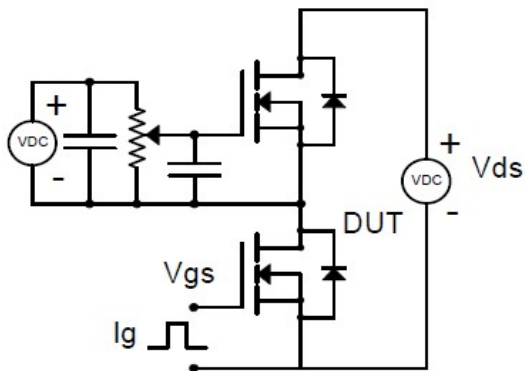
Figure9. Normalized Maximum Transient Thermal Impedance



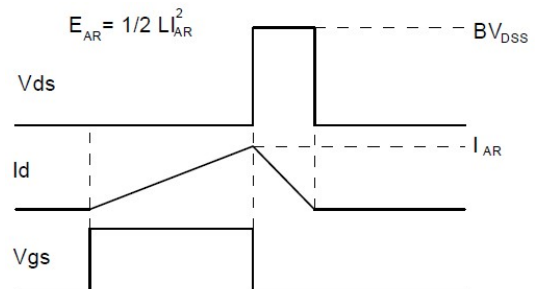
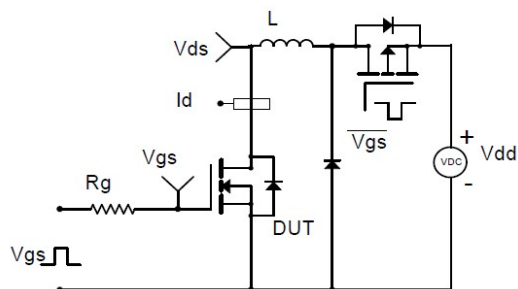
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Package Mechanical Data-SOP-8

